

100

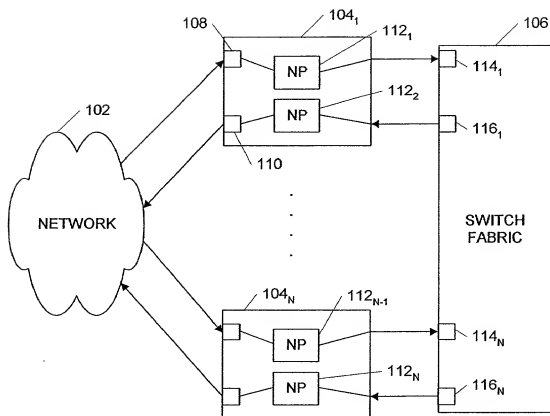


FIG. 1

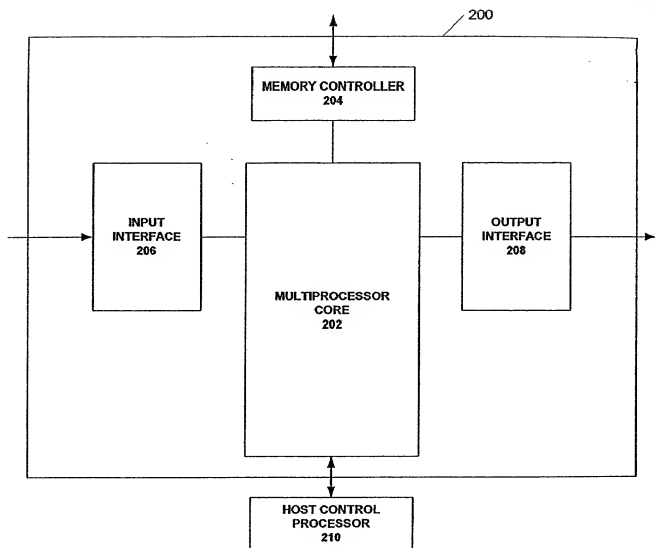
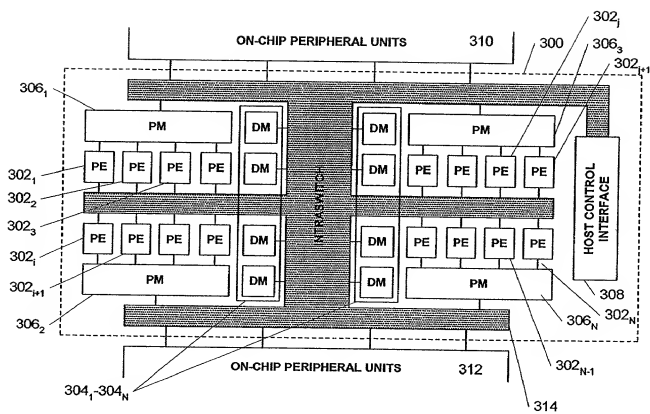


FIG. 2



PM: PROGRAM MEMORY
DM: DATA MEMORY
PE: PROCESSING ELEMENT

FIG. 3

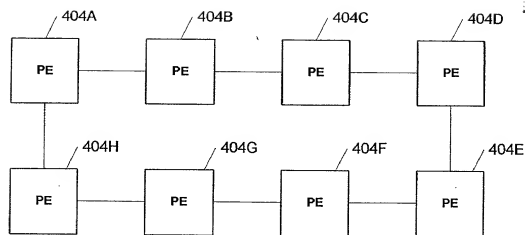


FIG. 4A

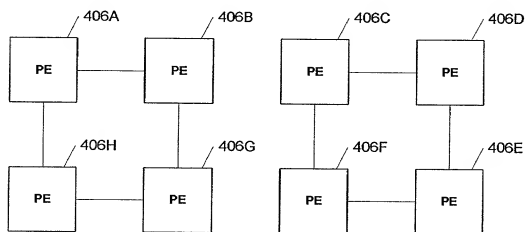


FIG. 4B

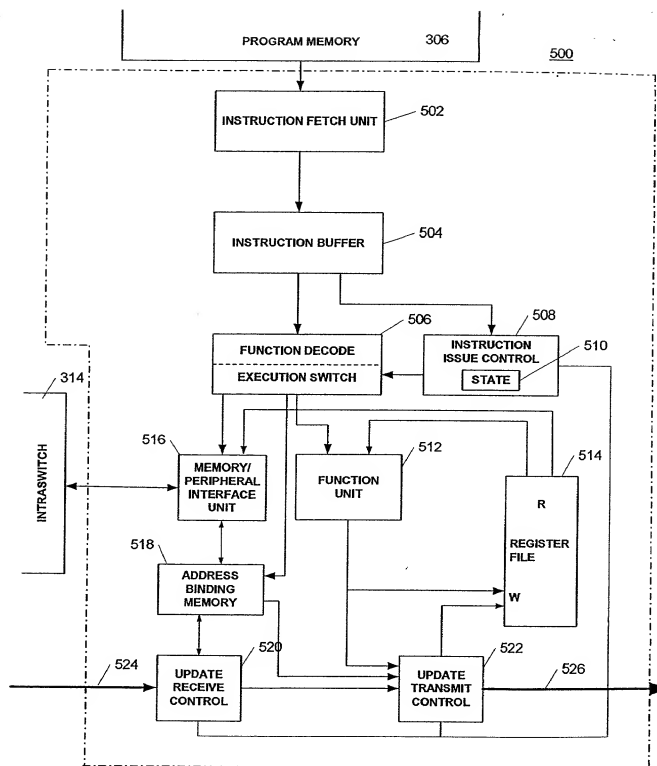


FIG. 5

600

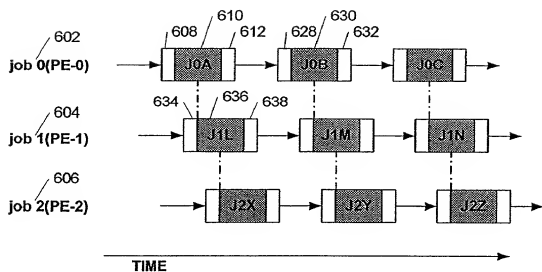


FIG. 6

700

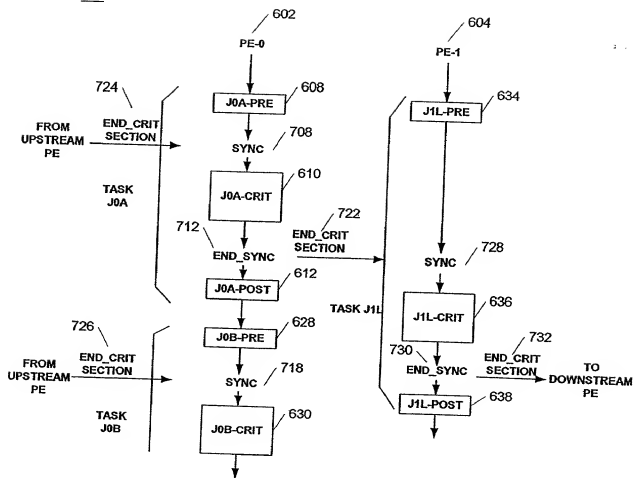


FIG. 7

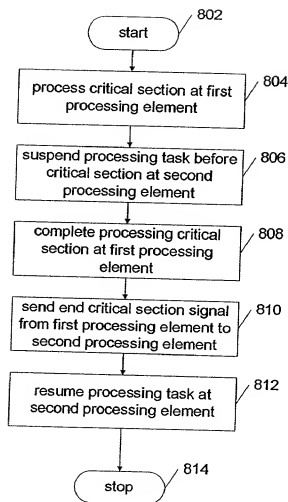


FIG. 8

900

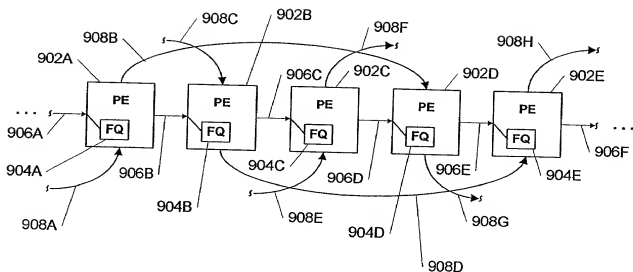
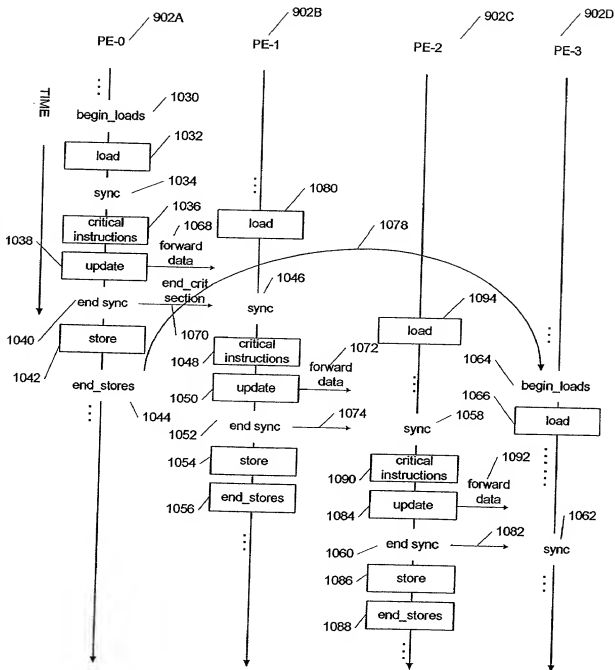


FIG. 9

FIG. 10



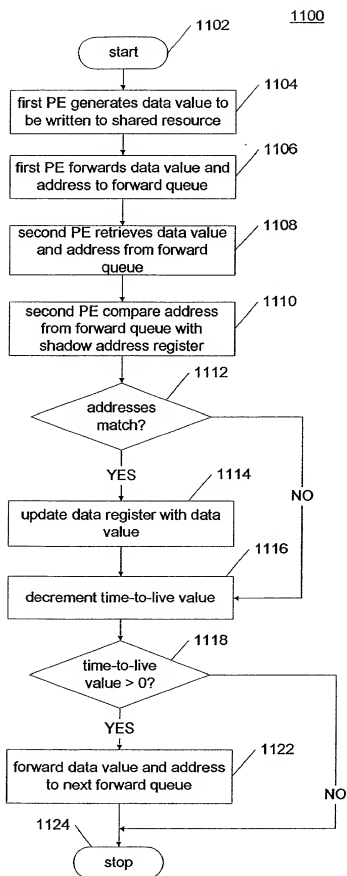


FIG. 11

1200

1212	1202	1204	1206	1208	1210
	DATA	ADDRESS	REGISTER #	TTL	LAST UPDATE
	D1	A1	R1	3	F
	D2	A2	R2	2	F
	D3	A3	R3	4	F
	D4	A4	R4	1	T

FIG. 12

1300

1302	1304	1306	1308	1310	1312	1314	1316
opcode	source 0	source 1	destination	update	sync	endstores	beginloads

FIG. 13